(Turn over)

1. Choose the correct answer of the following:

(a) Instruction Register
(b) Program Counter
(c) Data Register
(d) Address Register

2. During execution of a program, the register that keeps track of the next instruction is:

3. 2 x 10 = 20

4. Choose each correct answer of the following:

(a) Explain cache structure of Pentium.
(b) Explain cache structure of Pentium.
(c) Explain cache structure of Pentium.

5. Write short notes on any three of the following:

(a) What is MD5? How can it be used in trouble shooting of the system?
(b) Explain the various features of the 80186 processor.
(c) Explain the 8086 processor.

6. Discuss basic DMA operation with the help of diagram.

7. Explain cache structure of Pentium.

8. How is the memory system on the Pentium organized?

9. Does the 8086 CPU support generation indicating the sign?

GROUP A

Answer from both the groups as directed.

The figures in the margin indicate full marks. Your own words will not be acceptable.

Candidates are required to give their answers in full marks.

Time: 3 hours

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(2)

(i) 64K

(ii) 256

(iii) 1K

(iv) 1M

Control

The cycle required to fetch and execute
information is:

(i) Clock-cycle

(ii) Instruction cycle

(iii) Memory cycle

The 32-bit up carries data from or to the memory on 32-number:

(i) Address line

(ii) Data lines

(iii) Control lines

(iv) Input/liners

The up after completing the execution returns to:

(i) Halt state

(ii) Fetch-state

(iii) Execute-state

How many I/O addresses can the 80386 up access?

(i) 8-bit up

(ii) 16-bit up

(iii) 32-bit up

16-bit up

2.

(a) Explain the architecture of Intel

(b) Explain the PnP description of 8086 up for the maximum mode?

Group - B

(Long-answer type Questions)

15 x 4 = 60

8086 up

80266 up

8086

(i) 1 GB

(ii) 2 GB

(iii) 1 MB

(iv) None of these

Answer any four questions of the following:

(i) How many physical memory locations can the 80266 up have?

(ii) 24-bit

(iii) 20-bit

(iv) 16-bit

The 80386 up has the total address lines of:

(i) 32

(ii) 64

(iii) 36

(iv) None of these

The A0 - A3 address lines of 80357 DMA controller are:

(i) Inputs

(ii) Outputs

(iii) Bi-directional

(iv) None of these

Which up supports L2 cache?

(i) 8086

(ii) 80386

(iii) 80266

(iv) None of these

(Turnover)